REMARKS

Applicant respectfully requests reconsideration of this application as amended. Claims 1-5, 7-8, 10, 12-15 and 17-18 have been amended. Claims 6, 9, 11, 16, 19-21 and 24 have been cancelled without prejudice. No new claims have been added. Therefore, claims 1-5, 7-8, 10, 12-15, 17-18, 22-23 are presented for examination.

35 U.S.C. § 103 Rejection

Claims 1-4, 10-14 and 21 are rejected under 35 U.S.C. §103(a) as being unpatentable over Wolford, U.S. Patent No. 6,185,692 ("Wolford") in view of Lee et al., U.S. Patent No. 5,815,734 ("Lee).

Claim 1, as amended, recites:

> An apparatus, comprising:
> a variable speed bus; the variable speed bus initialized with a first clock frequency;
> a first unit coupled to the variable speed bus, the first unit having a first rate of requests to access the variable speed bus;
> a second unit coupled to the variable speed bus, the second unit having a second rate of requests to access the variable speed bus; and
> an arbitration and bus clock control unit to monitor the first access request rate from the first unit and the second access request from the second unit, and to determine a second clock frequency for the variable speed bus based on at least one of the first access rate and the second access request rate, wherein the arbitration and bus clock control unit to track a rate of request of the first and second units to access the variable speed bus, the arbitration and bus clock control unit is further to instruct a clock throttling logic to adjust a clock frequency associated with the variable speed bus according to bandwidth requirements of the first and second units based on the rate of request.
> (emphasis added)

Applicants respectfully disagree with the Examiner's characterization of the references and the pending claims; however, for the sake of expediting issuance of this

case, Applicants propose additional amendments to the pending claims and submit the following remarks.

Wolford discloses a "*data processing system includes a bus, one or more loads coupled to the bus, and a clock generator. The clock generator generates a bus clock signal that is coupled to at least one of the loads.* While the clock generator is generating a bus clock signal having a first frequency, the number of loads connected to the bus is determined. In response to this determination, the frequency of the bus clock signal is automatically changed from the first frequency to a second frequency. In one embodiment in which the bus is a PCI local bus having a plurality of slots, the determination of the number of loads is made by examining at least one storage location associated with each of a plurality of slots." (Abstract; emphasis added; see also Fig. 1, col. 3, lines 6-19, 37-42; col. 4, lines 6-12, 34-41, 62-66).

Wolford's changing the bus clock frequency based on the number of loads coupled to the bus whether the loads are active or idle is the same as having "**an arbitration and bus clock control unit to monitor the first access request rate from the first unit and the second access request from the second unit**, and to determine a second clock frequency for the variable speed bus based on at least one of the first access rate and the second access request rate, wherein the arbitration and bus clock control unit to track a rate of request of the first and second units to access the variable speed bus, **the arbitration and bus clock control unit is further to instruct a clock throttling logic to adjust a clock frequency associated with the variable speed bus according to bandwidth requirements of the first and second units based on the rate of request**" as recited by claim 1 (emphasis added).

The Examiner relies on Lee to make up for the deficiencies of the Wolford (page

3, Office Action, mailed 06-13-08). Lee discloses "facilitating operation of a peripheral bus, such as a PCI bus, at a higher clock frequency . . . If the system determines that the clock frequency will change due to a change in the system configuration (such as PCI devices being added or removed from the PCI bus), the configuration registers of each of the PCI devices can be modified to insure proper operation at the new clock frequency." (Abstract).

Referring now to a section relied upon by the Examiner, Lee discloses "[i]t should be understood, however, that more or less peripheral devices may be used, as desired and as permitted by the system specifications. Each of the peripheral devices 70, 80 preferably includes a status register 57, constructed and configured similarly to the status register of the BIU 50. In addition, each of the peripheral devices 70, 80 connects to the PCI bus 100 and to the CLK and 66 MHzENABLE lines, respectively . . . The clock driver 55 connects to the 66 MHzENABLE line to check the status of that line. If the 66 MHzENABLE line is asserted (i.e., pulled high), then the clock driver 55 drives the PCI bus clock signal at a frequency up to 66 MHz. Conversely, if the 66 MHzENABLE line is deasserted (i.e., drive low), the clock driver 55 drives the PCI bus clock signal at a frequency up to 33 MHz. Thus, in the preferred embodiment, the speed at which the PCI bus clock signal is driven by clock driver 55 is dependent on the status of the 66 MHzENABLE line." (col. 5, lines 31-59).

Nowhere does Lee discloses any of the feature of claim 1 to make up for the deficiencies of Wolford. For example, Wolford and Lee, neither individually nor when combined, teach or reasonably suggest an arbitration and bus clock control unit to monitor the first access request rate from the first unit and the second access request from the second unit, and to determine a second clock frequency for the variable speed bus

based on at least one of the first access rate and the second access request rate, wherein the arbitration and bus clock control unit to track a rate of request of the first and second units to access the variable speed bus, the arbitration and bus clock control unit is further to instruct a clock throttling logic to adjust a clock frequency associated with the variable speed bus according to bandwidth requirements of the first and second units based on the rate of request as recited by claim 1.

Furthermore, according to MPEP §2143, "[T]he Supreme Court in *KSR International Co. v. Teleflex, Inc.* 550 U.S. ___, ___, 82 USPQ2d 1395-1397 (2007) identified a number of rationales to support a conclusion of obviousness which are consistent with the proper "functional approach" to the determination of obviousness as laid down in *Graham.*" And, according to MPEP §2143.01, [o]bviousness can be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so. *In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1335 (Fed. Cir. 2006). Further, "[t]he mere fact that references can be combined or modified does not render the resultant combination obvious unless the results would have been predictable to one of ordinary skill in the art." *KSR International Co. v. Teleflex, Inc.* 550 U.S. ___, ___, 82 USPQ2d 1385, 1396 (2007).

Wolford and Lee, neither individually nor when combined, teach or reasonably suggest all the features of claim 1 and a *prima facie* case of obviousness has not been met under MPEP §2142. Accordingly, Applicant respectfully requests the withdrawal of the rejection of claim 1 and its dependent claims.

Claim 10 contains limitations similar to those of claim 1. Accordingly, Applicants respectfully request the withdrawal of the rejection of claim 10 and its

dependent claims.

35 U.S.C. § 103 Rejection

Claims 5, 7, 8, 15, 17 and 18 are rejected under 35 U.S.C. §103(a) as being unpatentable over Wolford in view of Lee and further in view of common knowledge in the data processing art at the time of the invention with and without the patent granted Keeley, U.S. Patent No. 5,844,794 ("Keeley").

Claims 5, 7, 8, 15, 17 and 18 depend from one of claims 1 and 10 and thus include all the limitations of the corresponding base claim. Accordingly, Applicants respectfully request the withdrawal of the rejection of claims 5, 7, 8, 15, 17 and 18.

Conclusion

In light of the foregoing, reconsideration and allowance of the claims is hereby earnestly requested.

Invitation for a Telephone Interview

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Request for an Extension of Time

Applicant respectfully petitions for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17(a) for such an extension.

Charge our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

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